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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,939	11/08/2001	Sheila M. Rader	CS11241	4806

23125 7590 10/20/2004

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,939	RADER, SHEILA M.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-18 and 20-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-11,13-18,20-25 and 35-38* is/are allowed.

6)☒ Claim(s) *1-3,5-8,26,29,32 and 33* is/are rejected.

7)☒ Claim(s) *4,27,28,30,31 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Amendment submitted on July 8, 2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 5-8, 26, 29 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (PGPUB: US 2002/0174311) in view of Eden (USPN: 6,611,537). Regarding claims 1, 3, 5-7, 26, 29 and 32-33, Ware discloses a virtual channel memory controller (Figures 27 and 31, Controller); a first memory device (Figure 27, Reference 2703) coupled to the virtual channel memory controller by a dedicated first bus (Figure 27, Reference 2708); a second memory device (Figure 27, Reference 2730) coupled to the virtual channel memory controller by a dedicated second data bus (Figure 27, Reference 2747); a shared address and control bus interconnecting the virtual channel memory controller and the first and second memory devices (Figure 31, Reference 3107). Ware does not explicitly disclose a DSP and RISC processor and a display controller coupled to virtual channel memory controller via a first DMA and second DMA channel, wherein the processors and the memory controller are integrated on a single circuit, synchronous memory devices and a communication system comprising the above features. Eden discloses a communication system (Figure 23) comprising

synchronous memory (Figure 23, Reference 5104), a DSP (DSP within Reference 5110 in Figure 23, refer to Figure 10, Reference 2150) and RISC processor (Figure 22, Reference 5002; Figure 23, Reference 5102) coupled via a first and second DMA channel (Figure 23, References 5146 and 5144) respectively to a memory controller (Figure 23, Reference 5112) and a display controller (Figure 23, Reference 5114) coupled to the memory controller wherein the DSP and the memory controller are located on a single integrated circuit (C 109, L 16-21). Memory systems are not stand-alone systems. They are used to store information for another device and thus it is evident that Ware's system is used in some type of processing system. Communication systems provide communication with other systems at high data speeds and hence it would have been obvious to one of ordinary skill in the art to use Ware's system in a communication system, such as the system taught by Eden, for the desirable purpose of providing high speed communication between two systems.

Regarding claims 8 and 29, Ware and Eden do not disclose the RISC processor integrated on the same circuit as the DSP processor and the memory controller. However, it is well known in the art to integrate system components on the same circuit to reduce delay times associated with communicating with off-chip circuitry. Hence, it would have been obvious to one of ordinary skill in the art to integrate the RISC processor on the same circuit with the DSP and memory controller for the desirable purpose of improved delay times.

4. Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Ware et al. (PGPUB: US 2002/0174311) in view of Eden (USPN: 6,611,537) as applied to claim 1 and further in view of Nain (USPN: 5,978,866).

Ware and Eden do not disclose the virtual memory channel controller having an address bus arbitration logic coupled to the first and second memories and a mutliplexer interconnecting the first and second memory devices to the shared address and control bus. However, Nain teaches the concept of a memory controller having an address bus arbitration logic coupled to the first and second memories and a mutliplexer interconnecting the first and second memory devices to the shared address and control bus (Figure 3, References 112 and 114; C 7, L 9-19). These features taught by Nain ensure proper operation of the bus via the arbitration logic and proper directing of information to a device from the shared bus via the multiplexer. It would have been obvious to one of ordinary skill in the art to include these features in the system taught by Ware and Eden for the desirable purpose of accuracy and to ensure proper bus operations.

Allowable Subject Matter

5. Claims 9-11, 13-18, 20-25 and 35-38 are allowed.

6. Claims 4, 27-28, 30-31 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

October 16, 2004